WHAT IS CLAIMED IS:

101. A transistor in a semiconductor device, comprising:

source/drain diffusion regions formed on a semiconductive region of a substrate; and

a transistor gate formed on the semiconductive region between the source/drain diffusion regions, the transistor gate extending in a vertical orientation from the substrate, the transistor gate comprising at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost layer having an insulated top surface.

102. The transistor of Claim 101, wherein the source/drain diffusion regions are elevated and extend in a vertical orientation from the substrate surface adjacent to the transistor gate.

103. The transistor of Claim 102, wherein each of the source/drain diffusion regions comprise at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost layer having an insulated top surface.

104. The transistor of Claim 103, wherein the source/drain diffusion regions comprise an uppermost epitaxial layer comprising a conductivity enhancing dopant.

105. The transistor of Claim 103, wherein each of the epitaxial layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

106. The transistor of Claim 101, wherein each epitaxial layer comprises a faceted top surface.

107. The transistor of Claim 101, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.

108. The transistor of Claim 101, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

109. The method of Claim 108, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

110. A transistor in a semiconductor device, comprising:

a transistor gate formed on a semiconductive region of a substrate; and

elevated source/drain diffusion regions formed on the semiconductive region adjacent to the transistor gate, and extending in a vertical plane from the substrate;

each of the source/drain diffusion regions covered by a layer of insulative material and comprising at least two overlying layers of epitaxially grown silicon.

111. The transistor of Claim 110, wherein the source/drain diffusion regions comprise an uppermost epitaxial layer comprising a conductivity enhancing dopant.

112. The transistor of Claim 110, wherein at least one of the epitaxial layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

113. The transistor of Claim 112, wherein at least one of the epitaxial layers comprises a concentration gradient of the dopant.

114. The transistor of Claim 110, wherein the epitaxial layers comprise a faceted top surface.

115. The transistor of Claim 110, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.

116. The transistor of Claim 110, wherein the transistor gate is covered by a layer of insulative material and comprises at least two overlying layers of epitaxially grown silicon.

Replacement Claims

117. A transistor in a semiconductor device, comprising:

a substrate having a buried drain region;

a gate overlying the buried drain region, the gate comprising multiple, vertically-oriented and overlying epitaxial layers and a top surface, each epitaxial layer having insulated sidewalls;

a source region overlying the top surface of the gate, the source region comprising an epitaxial layer doped with a conductivity enhancing dopant, and covered by a layer of insulative material.

118. The transistor of Claim 117, wherein each of the epitaxial layers of the gate is about 50 to about 200 nm thick.

119. The transistor of Claim 117, wherein the epitaxial layer of the source region is at least about 10 nm thick.

120. The transistor of Claim 117, wherein the epitaxial layers have a faceted top surface.

121. The transistor of Claim 117, wherein the buried drain comprises an n-type conductivity enhancing dopant an n-type selected from the group consisting of phosphine, arsine, and combinations thereof.

122. The transistor of Claim 117, wherein the buried drain region is about 50 nm to about 100 nm wide.

123. A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

an elevated source/drain diffusion region disposed on the substrate adjacent to the transistor gate in a vertical orientation from the substrate; the source/drain diffusion region comprising at least two overlying layers of epitaxially grown silicon; each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material, and the

uppermost epitaxial layer having a top surface with an overlying layer of an insulative material.

124. The transistor of Claim 123, wherein at least one of the epitaxial layers of the source/drain diffusion region comprises a conductivity enhancing dopant.

125. The transistor of Claim 124, wherein the uppermost epitaxial layer of the source/drain diffusion region comprises a conductivity enhancing dopant.

126. The transistor of Claim 124, wherein at least one of the epitaxial layers comprises a concentration gradient of the dopant.

127. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises a p-type dopant.

128. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises an n-type dopant.

129. (amended) A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

130. The semiconductor structure of Claim 129, wherein each epitaxial layer comprises a top surface defining a facet.

131. The semiconductor structure of Claim 130, wherein the facet has a (100) plane orientation.

132. The semiconductor structure of Claim 129, wherein each epitaxial layer has a thickness of up to about 200 nm.

133. The semiconductor structure of Claim 132, wherein each epitaxial layer has a thickness of about 50 to about 200 nm.

134. The semiconductor structure of Claim 132, wherein one or more epitaxial layers has a thickness of about 70 to about 100 nm.

135. The semiconductor structure of Claim 132, wherein each epitaxial layer has a thickness of at least about 10 nm to about 30 nm.

136. The semiconductor structure of Claim 129, being disposed adjacent to a gate or word line.

137. The semiconductor structure of Claim 129, being disposed adjacent to a source/drain region.

138. The semiconductor structure of Claim 137, being a transistor gate.

139. The semiconductor structure of Claim 138, wherein the transistor gate is isolated within the substrate by at least one dielectric isolation region disposed in the substrate adjacent thereto.

140. The semiconductor structure of Claim 129, being a source/drain diffusion region.

141. The semiconductor structure of Claim 140, wherein the uppermost epitaxial layer comprises a conductivity enhancing dopant.

142. The semiconductor structure of Claim 140, wherein each of the epitaxial layers comprises a conductivity enhancing dopant.

143. A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material, an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

144. The semiconductor structure of Claim 143, wherein the insulative layer comprises an oxide film, a nitride film, an oxidized nitride film, or a composite oxide/nitride film.

145. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon nitride film.

146. The semiconductor structure of Claim 145, wherein the silicon nitride film has a thickness of about 5 to about 20 nm.

147. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon oxide film.

148. The semiconductor structure of Claim 147, wherein the silicon oxide film has a thickness of about 2 to about 5 nm.

149. A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material; an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; one or more of the epitaxial layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

150. The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises a p-type dopant.

151. (amended) The semiconductor structure of Claim 150, wherein the p-type dopant is selected from the group consisting of diborane, boron trichloride, and boron trifluoride, and combinations thereof.

152. (amended) The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises an n-type dopant.

153. (amended) The semiconductor structure of Claim 152, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

154. (amended) The semiconductor structure of Claim 149, wherein one or more of the epitaxial layers comprises a concentration gradient of the dopant within the epitaxial layer.

155. (amended) The semiconductor structure of Claim 154, wherein the concentration gradient comprises a low to high concentration of the dopant within the epitaxial layer, with the high dopant concentration at the top surface of the layer.

156. (new) The semiconductor structure of Claim 129, being a component of a transistor.

157. (new) The semiconductor structure of Claim 156, being a transistor gate.

158. (new) The semiconductor structure of Claim 156, being a source/drain diffusion region.

159. (new) The semiconductor structure of Claim 158, wherein at least one of the epitaxial layers of the source/drain diffusion regions comprises a conductivity enhancing dopant.

160. (new) The semiconductor structure of Claim 159, wherein at least one of the epitaxial layers of the source/drain diffusion regions comprises a concentration gradient of a conductivity enhancing dopant.

161. (new) The semiconductor structure of Claim 157, wherein the transistor gate is disposed over a drain region disposed in the substrate.

162. (new) The semiconductor structure of Claim 161, the drain region is about 50 nm to about 100 nm wide.

163. (new) The semiconductor structure of Claim 161, wherein the uppermost epitaxial layer of the transistor gate structure comprises a source region doped with a conductivity enhancing dopant.

164. (new) The semiconductor structure of Claim 163, wherein the uppermost epitaxial layer is at least about 10 nm thick.

165. (new) The semiconductor structure of Claim 156, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

166. (new) The semiconductor structure of Claim 165, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

167. (new) The semiconductor structure of Claim 143, being a component of a transistor.

168. (new) The semiconductor structure of Claim 167, being a transistor gate.

169. (new) The semiconductor structure of Claim 167, being a source/drain diffusion region.

170. (new) The semiconductor structure of Claim 149, being a component of a transistor.

171. (new) The semiconductor structure of Claim 170, being a transistor gate.

172. (new) The semiconductor structure of Claim 170, being a source/drain diffusion region.

173. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

174. (new) The semiconductor structure of Claim 173, being a transistor gate.

175. (new) The semiconductor structure of Claim 173, being a source/drain diffusion region.

176. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material, an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

177. (new) The semiconductor structure of Claim 176, being a transistor gate.

178. (new) The semiconductor structure of Claim 176, being a source/drain diffusion region.

179. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material; an uppermost

epitaxial layer having a top surface with an overlying layer of an insulative material; one or more of the epitaxial layers comprising a conductivity enhancing dopant; the structure disposed on a substrate in a vertical orientation; and the structure being a component of a transistor.

180. (new) The semiconductor structure of Claim 179, being a transistor gate.

181. (new) The semiconductor structure of Claim 179, being a source/drain diffusion region.

182. (new) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and an uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

183. (new) The semiconductor device of Claim 182, comprising a transistor.

184. (new) The semiconductor device of Claim 183, wherein the structure comprises a transistor gate.

185. (new) The semiconductor device of Claim 183, wherein the structure comprises a source/drain diffusion region.

186. (new) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material, an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

187. (new) The semiconductor device of Claim 186, comprising a transistor.

188. (new) The semiconductor device of Claim 187, wherein the structure comprises a transistor gate.

189. (new) The semiconductor device of Claim 187, wherein the structure comprises a source/drain diffusion region.

190. (new) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxially grown silicon, each epitaxial layer having a top surface, and sidewalls with an overlying layer of an insulative material; an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; one or more of the epitaxial layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

191. (new) The semiconductor device of Claim 190, comprising a transistor.

192. (new) The semiconductor device of Claim 191, wherein the structure comprises a transistor gate.

193. (new) The semiconductor device of Claim 191, wherein the structure comprises a source/drain diffusion region.